CLAIMS

1. A method of using a system bus on a configurable system on a chip (CSoC), the CSoC including configurable system logic (CSL), the method comprising:

configuring a memory cell in the CSL using the system bus; and

reading the memory cell in the CSL using the system bus.

2. The method of Claim 1 wherein the system bus is controlled by a direct memory access (DMA) controller during the step of configuring.

3. The method of Claim 1 wherein the system bus is controlled by a central processing unit (CPU) during the steps of configuring and reading.

4. A method of initializing a configurable system on a chip (CSoC), the CSoC including configurable system logic (CSL), the method comprising:

selecting one of a plurality of clocks before configuring the CSL;

configuring the CSL; and

selecting one of the plurality of clocks after configuring the CSL.

5. A method of initializing a configurable system on a chip (CSoC), the CSoC including configurable system logic (CSL), the method comprising:

checking for one of a serial and a parallel output device external to the CSoC and coupled to a memory interface unit (MIU) in the CSoC;

setting the MIU to an appropriate mode based on the output device;

searching for a header in the output device;

switching to another mode if the header is not found; and

configuring the CSL if the header is found.

6. The method of Claim 5, wherein if the header is not found in the other mode, then further including:

checking whether the output device is accessible;

powering down the CSoC if the output device is accessible; and

repeating the steps in Claim 5 if the output device is not accessible.

7. A programmable interconnect structure providing a signal to a logic block, the interconnect structure comprising:

a plurality of interconnect lines divided into sets of interconnect lines;

a plurality of first-tier multiplexers, each first-tier multiplexer having input terminals coupled to a set of interconnect lines and having an output terminal;

a plurality of second-tier multiplexers, each second-tier having a first input terminal coupled to one output terminal of the first-tier multiplexers and a second input terminal coupled to a constant voltage source,

wherein the plurality of second-tier multiplexers selectively provide output signals from the first terminals or the second terminals to the logic block.

8. A method of providing signals to a logic block, the method comprising:

selectively providing one of a plurality of interconnect signals and a constant logic signal to the logic block,

wherein during a configuration mode, the constant logic signal is provided to the logic block, and

wherein during a user mode, the plurality of interconnect signals are provided to the logic block.

9. An input multiplexer to a logic block, the input multiplexer comprising:

a first multiplexer receiving a first plurality of input signals and a constant signal;

a second multiplexer receiving a second plurality of input signals and a mode signal;

a third multiplexer receiving output signals from the first and second multiplexers and providing an output signal on a logic block input line; and

a first transistor coupled to an internal logic block line, the first transistor controlled by the mode signal.

10. A method of providing signals on an internal logic block line of a logic block, the method comprising:

providing a plurality of input signals to a plurality of selectors, wherein each selector further receives one of a constant logic value and a mode signal;

selectively providing one of the plurality of input signals, the constant logic value, and the mode signal on the internal logic block line, wherein the mode signal indicates whether the logic block is in a configuration mode or a user mode.

11. The method of Claim 10, wherein during configuration, the plurality of input signals, the constant logic value, and the mode signal have the same value.

12. The method of Claim 10, wherein during the user mode, the constant logic value and the mode signal have different values.

13. The method of Claim 10, further including using the mode signal to transfer the constant logic value to the internal logic block line.

Practioner's Docket No. TRI[redacted]

PATENT

COMBINED DECLARATION AND POWER OF ATTORNEY

(ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL, DIVISIONAL, CONTINUATION, OR C-I-P)

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is for an original application.

INVENTORSHIP IDENTIFICATION

My residence, post office address and citizenship are as stated below, next to my name. I believe that I am the original, first and sole inventor *(if only one name is listed below)* or an original, first and joint inventor *(if plural names are listed below)* of the subject matter that is claimed, and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

"Configuration In A Configurable System On A Chip"

SPECIFICATION IDENTIFICATION

In re application of: Brian Fox and Andreas Papaliolios
Serial No. 09/419,386
Filed on: 10/15/1999

ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in 37, Code of Federal Regulations, §1.56, and which is material to the examination of this application, namely, information where there is a substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent.

POWER OF ATTORNEY

I hereby appoint the following practitioners to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Patrick T. Bever	Registration Number 33,834
E. Eric Hoffman	Registration Number 38,186
Jeanette S. Harms	Registration Number 35,537
Edward S. Mao	Registration Number 40,713
Julie A. Stephenson	Registration Number 41,330

SEND CORRESPONDENCE TO

Jeanette S. Harms, Esq.
BEVER & HOFFMAN, LLP
2099 Gateway Place, Suite 320
San Jose, CA 95110-1017

DIRECT TELEPHONE CALLS TO:

(408) 451-5907

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(S)

Brian Fox
Inventor's signature _____
Date 11/18/99 **Country of Citizenship** United States
Residence Sunnyvale, CA
Post Office Address 1414 Mallard Way
Sunnyvale, CA 94087

Andreas Papaliolios
Inventor's signature _____
Date 24 Nov 99 **Country of Citizenship** United States
Residence Sunnyvale, CA
Post Office Address 1338 Torrance Avenue
Sunnyvale, CA 94089